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DATA SHEET

CBT3245A
Octal bus switch

Product data
Supersedes data of 2002 Feb 18

2003 Jun 27

Philips
Semiconductors

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Octal bus switch CBT3245A

FEATURES

- Standard ’245-type pinout
- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), thin shrink small outline (TSSOP)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT3245A provides eight bits of high-speed TTL-compatible bus switching in a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3245A device is organized as one 8-bit switch. When enable ($\overline{OE}$) is LOW, the switch is on and port A is connected to port B. When $\overline{OE}$ is HIGH, the switch is open and a high-impedance state exists between the two ports.

The CBT3245A is characterized for operation from -40 to +85 °C.

PIN CONFIGURATION — SO, SSOP, QSOP, AND TSSOP

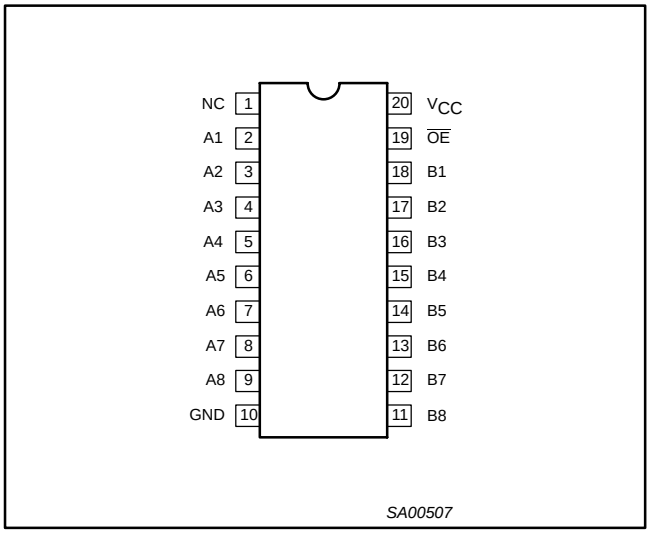


Figure 1. Pin configuration — SO, SSOP, QSOP, and TSSOP

PIN CONFIGURATION — DHVQFN

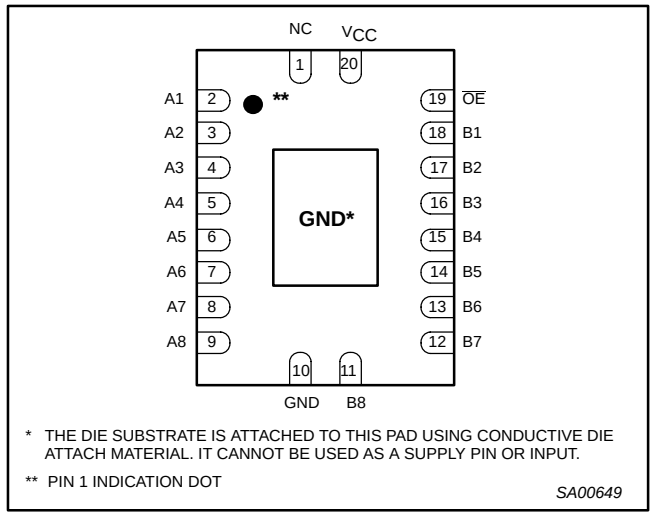


Figure 2. Pin configuration — DHVQFN (top view)

PIN DESCRIPTION

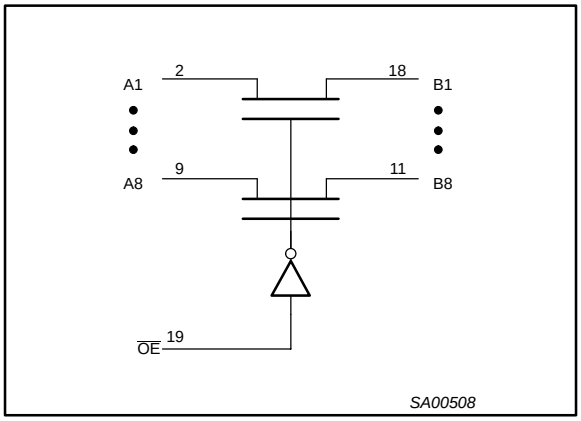
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	NC	No internal connection
19	$\overline{OE}$	Output enable input
2, 3, 4, 5, 6, 7, 8, 9	A1-A8	Inputs
18, 17, 16, 15, 14, 13, 12, 11	B1-B8	Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
20-Pin Plastic DHVQFN	-40 to 85 °C	CBT3245ABQ	CT3245A	SOT764-1
20-Pin Plastic TSSOP	-40 to 85 °C	CBT3245APW	CT3245A	SOT360-1
20-Pin Plastic SSOP (QSOP)	-40 to 85 °C	CBT3245ADS	CT3245ADS	SOT724-1
20-Pin Plastic SSOP	-40 to 85 °C	CBT3245ADB	CT3245A	SOT339-1
20-Pin Plastic SO	-40 to 85 °C	CBT3245AD	CBT3245AD	SOT163-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

LOGIC SYMBOL



FUNCTION TABLE

INPUT	INPUTS/OUTPUTS
$\overline{OE}$	A, B
L	A = B
H	Z

H = HIGH voltage level
L = LOW voltage level
Z = HIGH impedance “off” state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	-0.5 to +7	V
I_{OUT}	DC output current	output in LOW state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	—	V
V_{IL}	LOW-level input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = -40 to +85 °C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = -18 mA	—	—	-1.2	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	—	—	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND	—	1	3	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	3.5	mA
C_I	Control pins	V_I= 3 V or 0, $\overline{OE}$ = V_{CC}	—	3.2	—	pF
$C_{IO(OFF)}$	Pin capacitance (OFF state)	V_O = 3 V or 0	—	6.6	—	pF
r_{on}[3]	On-resistance	V_{CC} = 4.5 V; V_1 = 0 V; I_I = 64 mA	—	5	7	Ω
		V_{CC} = 4.5 V; V_1 = 0 V; I_I = 30 mA	—	5	7	
		V_{CC} = 4.5 V; V_1 = 2.4 V; I_I = 15 mA	—	10	15	

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

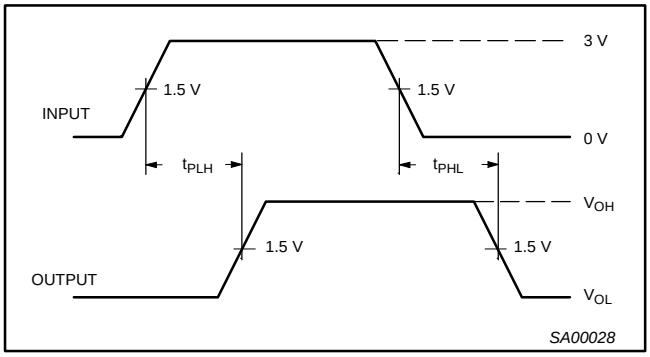
GND = 0 V; t_R; C_L = 50 pF

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CBT3245A		UNIT
				T_{amb} = -40 to +85 °C V_{CC} = +5.0 V ±0.5 V		
				MIN	MAX	
t_{pd}	Propagation delay[1]	A or B	B or A	—	0.25	ns
t_{en}	Output enable time to HIGH and LOW level	$\overline{OE}$	A or B	1.0	5.9	ns
t_{dis}	Output disable time from HIGH and LOW level	$\overline{OE}$	A or B	1.0	6.0	ns

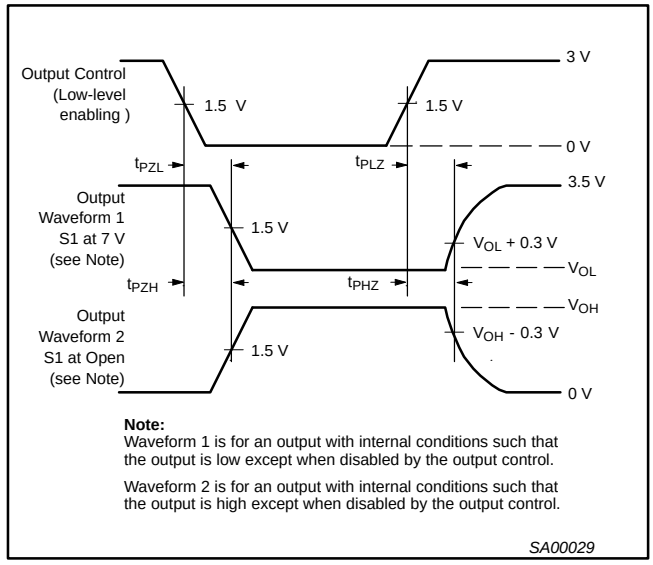
NOTES:
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V

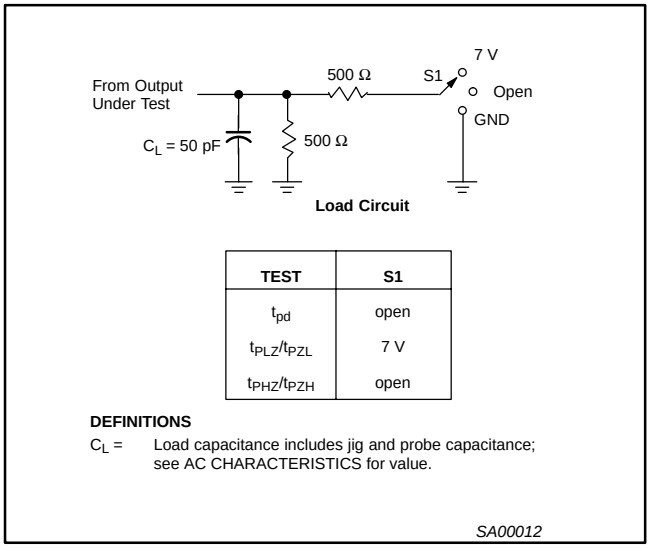


Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

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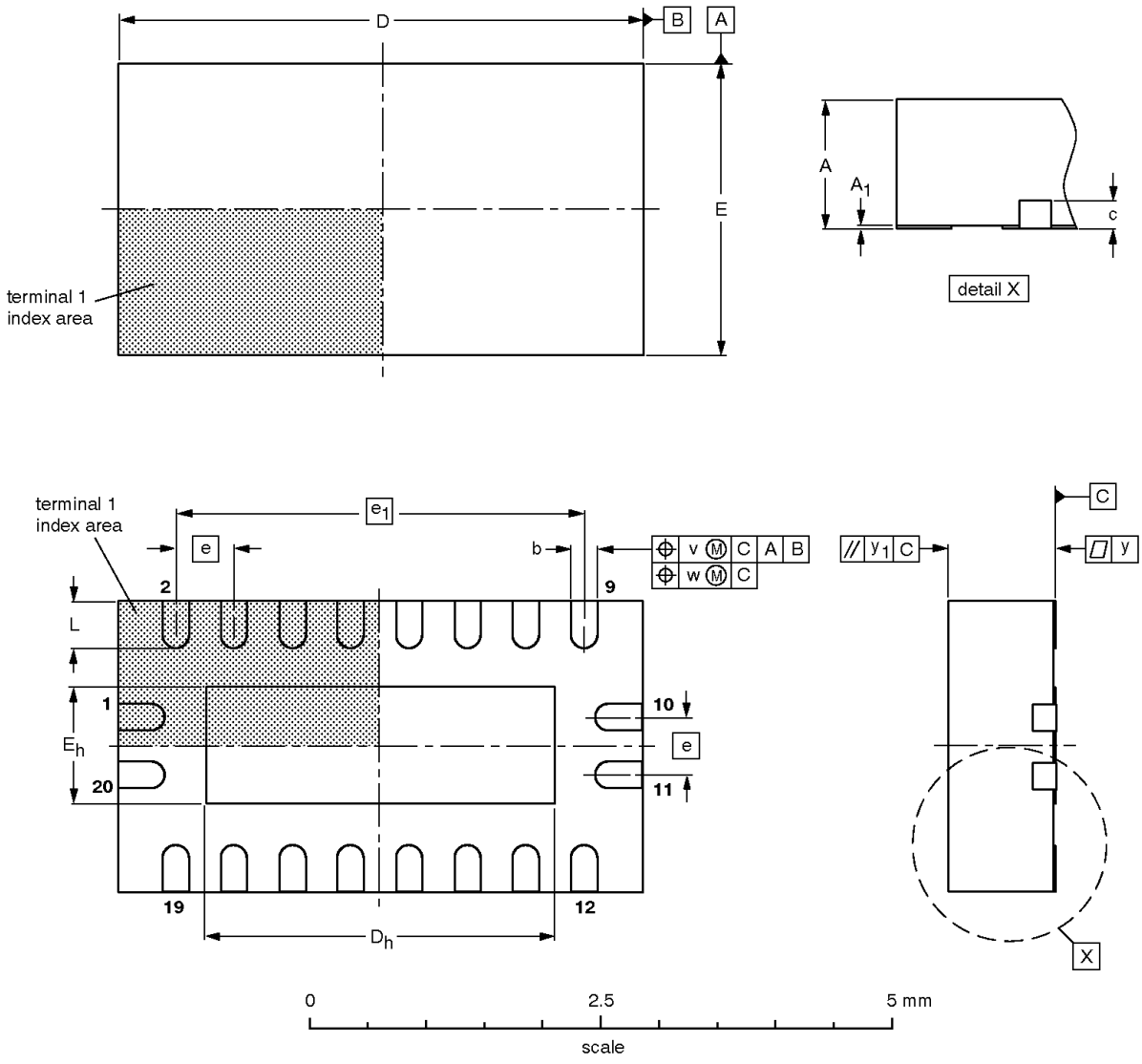
NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

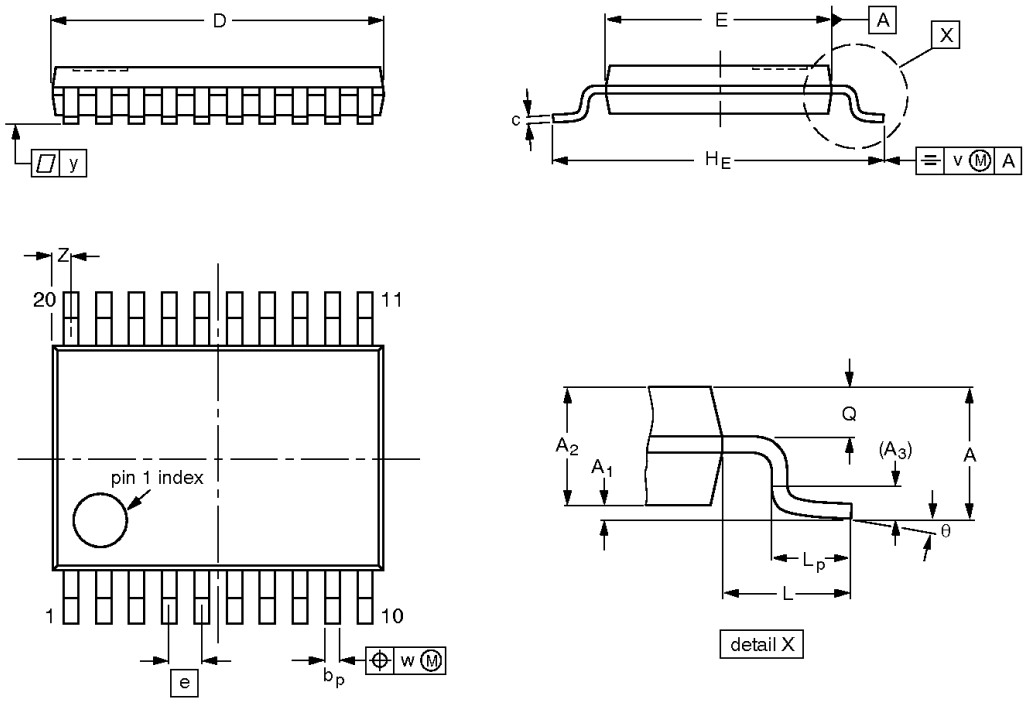
UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

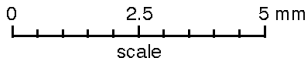
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm SOT360-1





DIMENSIONS (mm are the original dimensions)

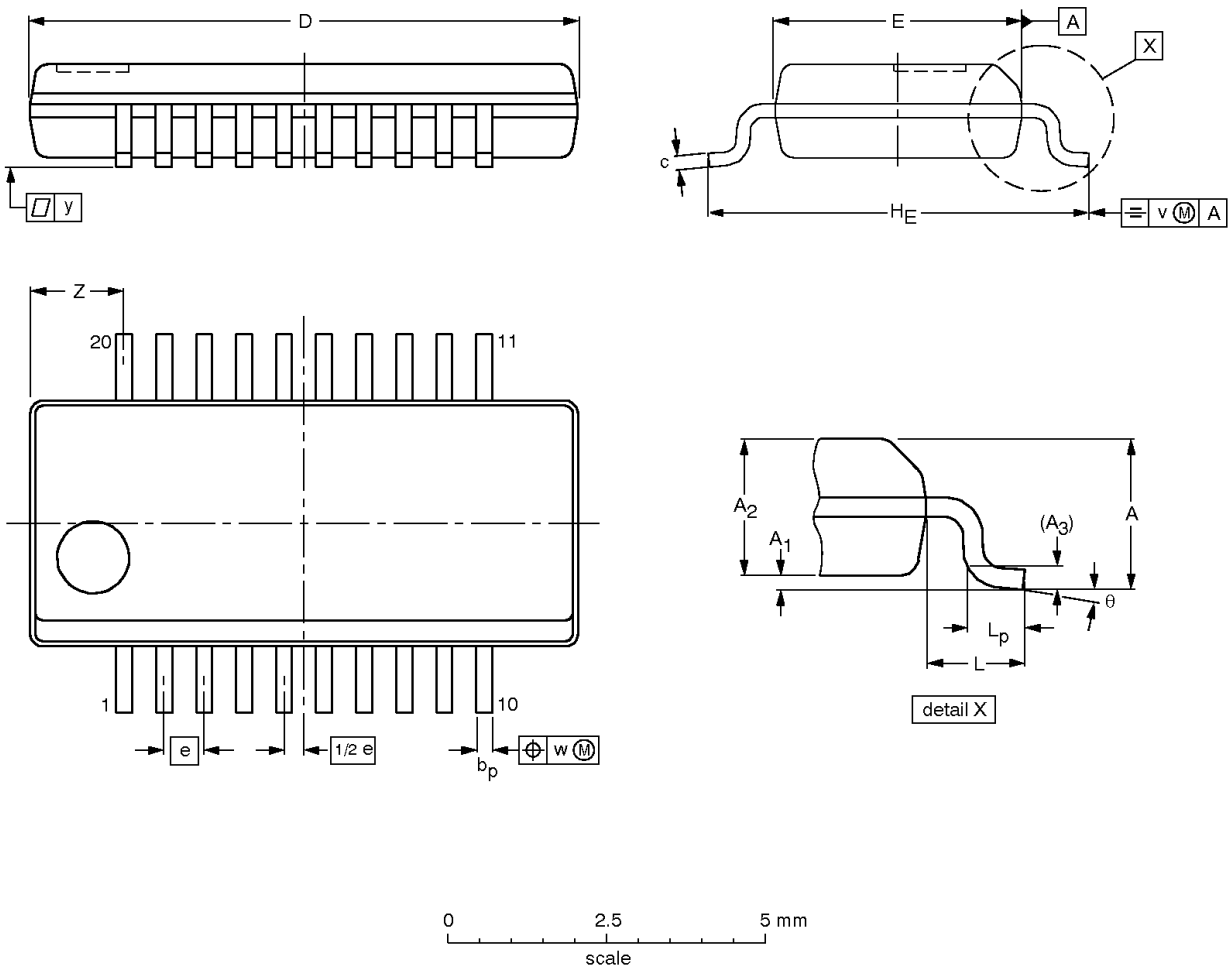
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT724-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

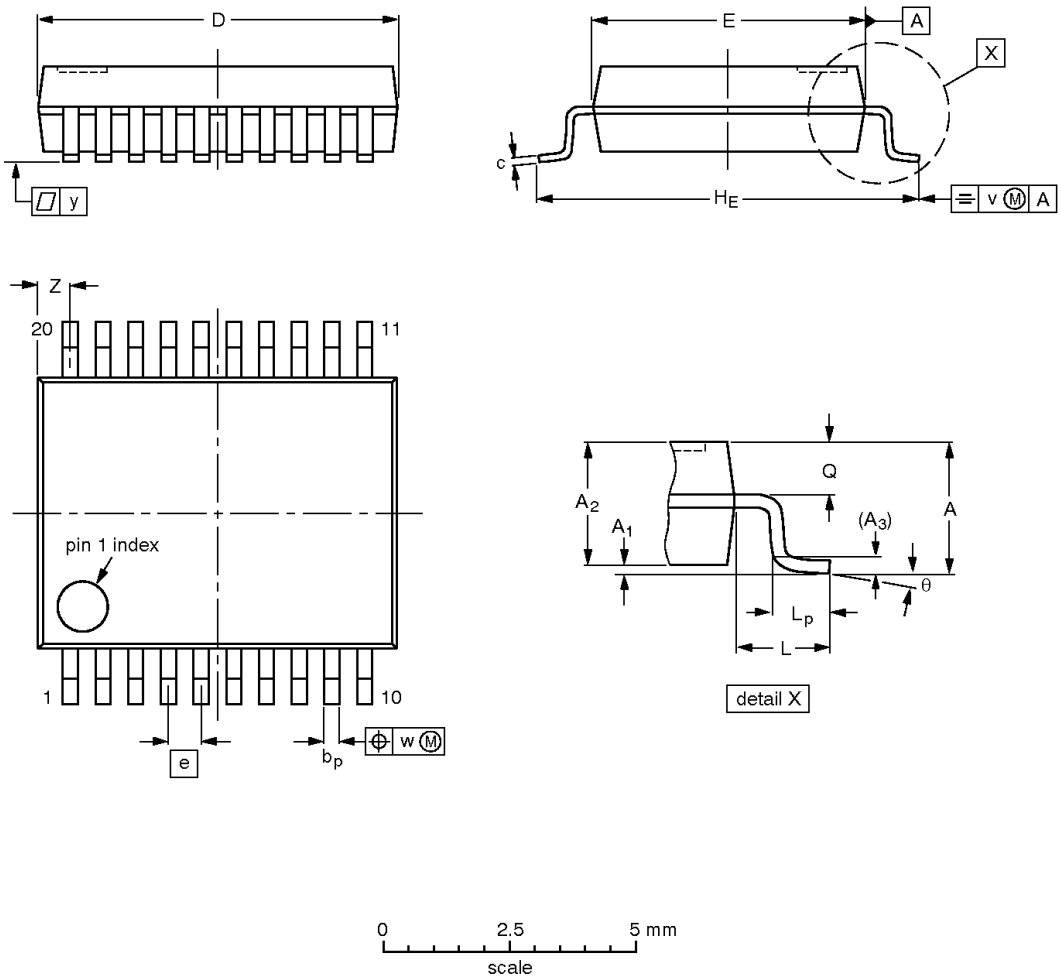
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.25	0.18	0.1	1.67 1.28	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT724-1		MO-137				~~01-07-04~~ 03-02-18

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

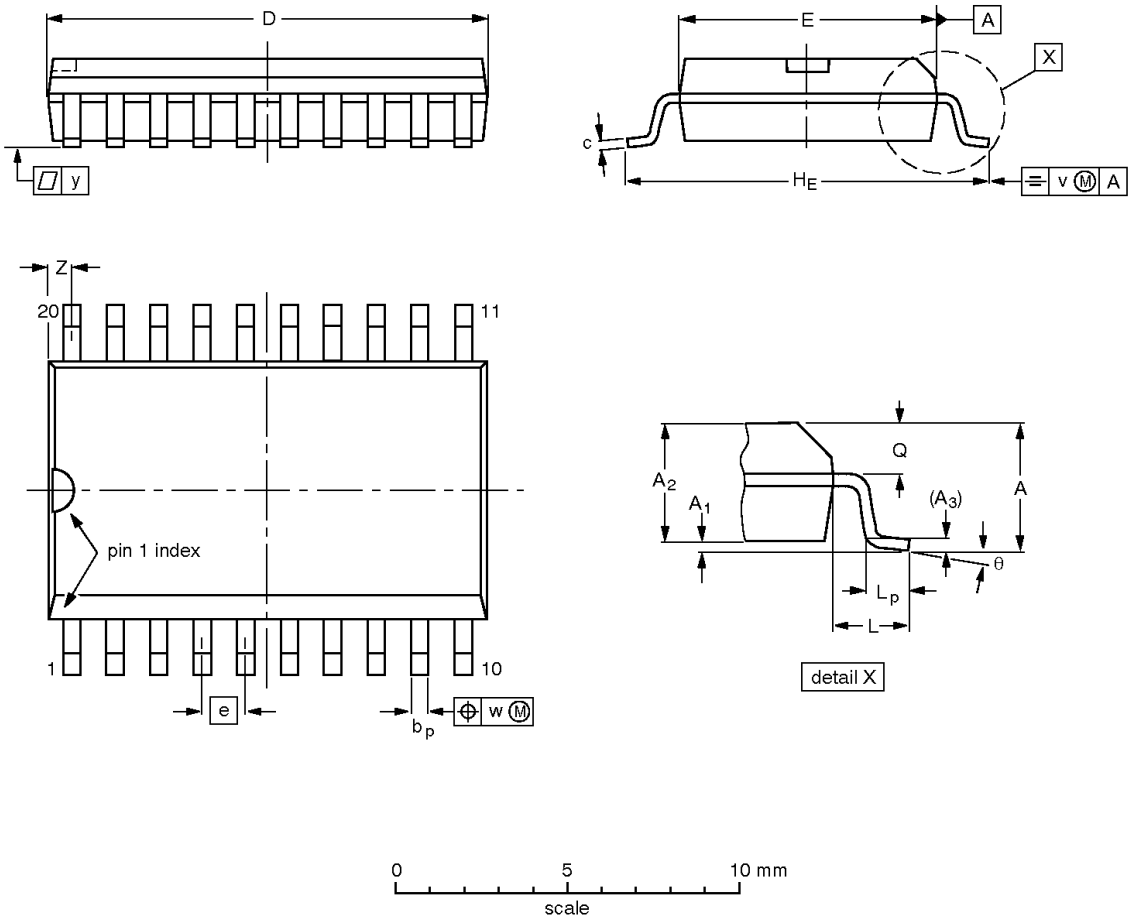
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_2	20030627	**Product data (9397 750 11679); ECN 853-2313 30017 dated 11 Jun 2003. Supersedes data of 2002 Feb 18 (9397 750 09462).** Modifications: • Addition of QSOP and DHVQFN package types.
_1	20020218	Product data (9397 750 09462); ECN 853-2313 27745 of 18 Feb 2002.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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